In The Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A buffer circuit comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and wherein the first logic gate includes a plurality of serially connected transistors in an electrical path between the supply voltage and the first output node; and

a second logic gate configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal and wherein the second logic gate includes a plurality of serially connected transistors in a path between the supply voltage and the second output node;

wherein the number of serially connected transistors in the path between the supply voltage and the first output node is equivalent to the number of serially connected transistors in the path between the supply voltage and the second output node;

<u>wherein the plurality of serially connected transistors in the electrical path between the supply voltage and the first output node comprises a first transistor having a first control electrode connected to the data signal and a second transistor coupled in series between the supply voltage and the first transistor, the first logic gate further comprising a third transistor</u>

connected in parallel with the first transistor between the second transistor and the first output node, wherein the third transistor has a third control electrode connected to the control signal.

Claim 2 (canceled).

3. (currently amended) A buffer circuit according to ~~Claim 2~~ Claim 1 wherein each of the first, second, and third transistors have a same conductivity type.

4. (currently amended) A buffer circuit according to ~~Claim 2~~ Claim 1 wherein the first transistor is a first PMOS transistor, wherein the second transistor is a second PMOS transistor, and wherein the third transistor is a third PMOS transistor.

5. (original) A buffer circuit according to Claim 4 wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are PMOS transistors.

6. (original) A buffer circuit according to Claim 4, the first logic gate further comprising a plurality of serially connected NMOS transistors between the first output node and the reference voltage, the plurality of serially connected NMOS transistors including a first NMOS transistor having a first NMOS control electrode connected to the data signal and a second NMOS transistor having a second NMOS control electrode connected to the control signal.

7. (currently amended) A buffer circuit according to Claim 6, the first logic gate further comprising a third NMOS transistor connected ~~with the first output node~~ in parallel with the first NMOS transistor between the first output node and the second NMOS transistor, the third NMOS transistor having a third NMOS control electrode connected to the reference voltage.

8. (currently amended) A buffer circuit according to ~~Claim 2~~ Claim 1 wherein the first and second logic gates are further responsive to a second control signal, the first logic gate

further comprising a fourth transistor connected in parallel with the first and third transistors between the second transistor and the first output node, the fourth transistor having a control electrode connected to the second control signal.

9. (original) A buffer circuit according to Claim 8, the first logic gate further comprising a fifth transistor connected in series with the second transistor between the first transistor and the supply voltage.

10. (original) A buffer circuit according to Claim 1 wherein the reference voltage comprises a ground voltage.

11. (original) A buffer circuit according to Claim 1 wherein the first logic gate comprises a NAND gate and wherein the second logic gate comprises a NOR gate.

12. (original) A buffer circuit according to Claim 1 wherein the plurality of serially connected transistors in the path between the supply voltage and the first output node are PMOS transistors, and wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are PMOS transistors.

13. (currently amended) An output buffer comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and wherein the first logic gate includes a

plurality of serially connected transistors in a path between the first output node and the reference voltage; and

a second logic gate configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal and wherein the second logic gate includes a plurality of serially connected transistors in a path between the second output node and the reference voltage;

wherein the number of serially connected transistors in the path between the first output node and the reference voltage is equivalent to the number of serially connected transistors in the path between the second output node and the reference voltage;

wherein the plurality of serially connected transistors in the electrical path between the second output node and the reference voltage comprises a first transistor having a first control electrode connected to the data signal and a second transistor connected in series between the first transistor and the reference voltage, the second logic gate further comprising a third transistor connected in parallel with the first transistor between the second transistor and the second output node, wherein the third transistor has a control electrode connected to the inverse of the control signal.

Claim 14 (canceled).

15. (currently amended) A buffer circuit according to ~~Claim 14~~ Claim 13 wherein each of the first, second and third transistors have a same conductivity type.

16. (currently amended) A buffer circuit according to ~~Claim 14~~ Claim 13 wherein the first transistor is a first NMOS transistor, wherein the second transistor is a second NMOS transistor, and wherein the third transistor is a third NMOS transistor.

17. (original) A buffer circuit according to Claim 16 wherein the plurality of serially connected transistors in the path between the first output node and the reference voltage are NMOS transistors.

18. (original) A buffer circuit according to Claim 16, the second logic gate further comprising a plurality of serially connected PMOS transistors between the supply voltage and the second output node, the plurality of serially connected PMOS transistors including a first PMOS transistor having a first PMOS control electrode connected to the data signal and a second PMOS transistor having a second PMOS control electrode connected to the inverse of the control signal.

19. (currently amended) A buffer circuit according to Claim 18, the second logic gate further comprising a third PMOS transistor connected ~~with the second output node~~ in parallel with the first PMOS transistor between the second PMOS transistor and the second output node, the third PMOS transistor having a third PMOS control electrode connected to the supply voltage.

20. (currently amended) A buffer circuit according to ~~Claim 14~~ Claim 13 wherein the first and second logic gates are further responsive to a second control signal, the second logic gate further comprising a fourth transistor connected in parallel with the first and third transistors between the second transistor and the second output node, the fourth transistor having a control electrode connected to an inverse of the second control signal.

21. (original) A buffer circuit according to Claim 20, the second logic gate further comprising a fifth transistor connected in series with the second transistor between the first transistor and the reference voltage.

22. (original) A buffer circuit according to Claim 13 wherein the reference voltage comprises a ground voltage.

23. (original) A buffer circuit according to Claim 13 wherein the first logic gate comprises a NAND gate and wherein the second logic gate comprises a NOR gate.

24. (original) A buffer circuit according to Claim 13 wherein the plurality of serially connected transistors in the path between the first output node and the reference voltage are NMOS transistors, and wherein the plurality of serially connected transistors in the path between the second output node and the reference voltage are NMOS transistors.

Claims 25-40 (canceled).

41. (currently amended) An output buffer circuit comprising:

a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives at least one control signal and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the control signal and the data and generates the pull-down control signal,

wherein ~~the~~ a number of PMOS transistors present along ~~the~~ a path of a first supply voltage to an output terminal of the NAND gate is equivalent to ~~the~~ a number of PMOS transistors present along ~~the~~ a path of the first supply voltage to an output terminal of the NOR gate, and ~~the~~ a number of NMOS transistors present along ~~the~~ a path of a second supply voltage to an output terminal of the NAND gate is equivalent to ~~the~~ a number of NMOS transistors present along ~~the~~ a path of the second supply voltage to an output terminal of the NOR gate.

42. (original) The output buffer circuit of claim 41, wherein the NAND gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the second supply voltage is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a third PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input; and

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor, a gate to which the control signal is applied, and a source to which the second supply voltage is applied.

43. (original) The output buffer circuit of claim 41, wherein the NOR gate includes:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the inverted signal of the control signal is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NOR gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the inverted signal of the control signal is applied;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is input; and

a third NMOS transistor which has a drain connected to sources of the first and second NMOS transistors, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

44. (original) The output buffer circuit of claim 42, wherein the NAND gate further comprises a third NMOS transistor which has a drain connected to the output terminal of the

NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

45. (original) The output buffer circuit of claim 43, wherein the NOR gate further comprises a third PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.

46. (original) The output buffer circuit of claim 41, wherein the NAND gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the second supply voltage is applied;

a second PMOS transistor which has a source connected to the drain of the first PMOS transistor and a gate to which the second supply voltage is applied;

a third PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a fourth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which a first control signal is applied, and a drain connected to the output terminal of the NAND gate;

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which a second control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor and a gate to which the first control signal is applied; and

a third NMOS transistor which has a drain connected to a source of the second NMOS transistor, a gate to which the second control signal is applied, and a source to which the second supply voltage is applied.

47. (original) The output buffer circuit of claim 41, wherein the NOR gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the data is input;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor and a gate to which an inverted signal of the first control signal is applied;

a third PMOS transistor which has a source connected to a drain of the second PMOS transistor, a gate to which an inverted signal of the second control signal is applied, and a drain connected to the output terminal of the NOR gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which an inverted signal of the first control signal is applied;

a third NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which an inverted signal of the second control signal is applied;

a fourth NMOS transistor which has a drain connected to sources of the first through third NMOS transistors and a gate to which the first supply voltage is applied; and

a fifth NMOS transistor which has a drain connected to a source of the fourth NMOS transistor, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

48. (original) The output buffer circuit of claim 46, wherein the NAND gate comprises a fourth NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor; and

a fifth NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

49. (original) The output buffer circuit of claim 47, wherein the NOR gate further comprises:

a fourth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate; and

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.

Claims 50-55 (canceled).